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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,759	12/16/2003	Kazuhiro Yoshida	36856.1185	3349
7590	04/27/2005			EXAMINER TRINH, HOA B
Keating & Bennett LLP Suite 312 10400 Eaton Place Fairfax, VA 22030			ART UNIT 2814	PAPER NUMBER

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/735,759	YOSHIDA, KAZUHIRO
	Examiner Vikki H. Trinh	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 01 April 2005.
- 2a) This action is **FINAL**.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-13 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 16 December 2003 is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_\_

## DETAILED ACTION

### Claims Status

Claims 1-13 are pending in this present application.

#### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.
2. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:
  1. Determining the scope and contents of the prior art.
  2. Ascertaining the differences between the prior art and the claims at issue.
  3. Resolving the level of ordinary skill in the pertinent art.
  4. Considering objective evidence present in the application indicating obviousness or nonobviousness.
3. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosoya (JP 08-340213) in view of Nakamura et al. (5,438,218) (hereinafter Nakamura).

Hosoya discloses a semiconductor device having a semiconductor substrate 1 (abstract) ; a field effect transistor 11 (abstract) provided on the semiconductor

substrate 11 (abstract) and having electrodes 6, 7, 8, 9 and 10 (abstract), the transistor 11 (abstract) having a gate recess (fig. 1; abstract) and a Schottky junction (fig. 1) for a gate electrode 5 (fig. 1), and a diode 12 (fig. 1) provided on the semiconductor substrate 1 (fig. 1) and having electrodes 9,10 (fig. 1), the diode 12 (fig. 1) having an n-type layer 4; wherein at least one of the electrodes 6, 7 (fig. 1) of the field effect transistor and at least one of the electrodes of the diode 9, 10 (fig. 1) are composed of metal conductors which are simultaneously formed. Note that the preamble of the present claim states a device, thereby the formation process of the conductive layers have been considered but they are not structurally distinguished over the prior art of record.

However, Hosoya does not explicitly disclose that the diode is a pn junction diode having a p-type layer and an n-type layer.

Nakamura discloses an analogous semiconductor device, the device (fig. 11D and fig. 12) having a pn junction diode (col. 4, lines 14-15; fig. 11D) with a p-type layer 306 and an n-type layer 303 (col. 4, lines 20-21). The diode includes a cathode and an anode (col. 4, lines 4-8; and col. 3, lines 65-68). Further, the device includes at least one ion implanted region 304, 302 (fig. 11D) disposed between the field effect transistor 309 (fig. 11D) and the pn junction (fig. 11D).

Therefore, as to claims 1 and 8, it would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Hosoya with the pn diode having a p-type layer and an n-type layer and at least one ion implanted region, as taught by Nakamura, so as to improve the breakdown voltage of the diode (Nakamura, col. 1, lines 25-27)

As to claims 2, 9, Hosoya discloses a source electrode 6 (fig. 1) and a drain electrode 7 (fig. 1) of the field effect transistor 11 (fig. 1) and a cathode 9 (fig. 1) of the diode are composed of metal conductors. Note that the preamble of the present claim states a device, thereby the formation process of the conductive layers have been considered but they are not structurally distinguished over the prior art of record.

As to claims 3, 10, Hosoya discloses the gate electrode 5 (fig. 1) of the field effect transistor 11 (fig. 1) and an anode 10 (fig. 1) of the diode are composed of metal conductors. Note that the preamble of the present claim states a device, thereby the formation process of the conductive layers have been considered but they are not structurally distinguished over the prior art of record.

As to claims 4,11, Hosoya discloses at least one of active layers 2, 3, 4 (abstract) of the field effect transistor 11 (abstract) and at least one of active layers

2, 3, 4 (fig. 1) of the diode are composed of layers which are obtained from a common active layer 4 (fig. 1) which is epitaxially grown.

As to claims 5, 12, Hosoya discloses contact layers 2, 3, 4 (fig. 1) of the field effect transistor 11 (fig. 1) and of the n-type layer 4 (fig. 1) of the diode 12 (fig. 1) are composed of layers 2, 3, 4 (fig. 1) which are obtained from a common n-type layer 4 (fig. 1) provided on the semiconductor substrate 1 (fig. 1) which is epitaxially grown.

As to claim 6, Hosoya discloses the contact layers 2, 3, 4 (fig. 1) are provided on a channel layer 4 (fig. 1) on the semiconductor substrate 1 (fig. 1) of the field effect 11 (fig. 1), and Nakamura discloses the p-type layer 306 (fig. 11D) of the pn junction diode (fig. 11D) being over the n-type layer 303 (fig. 11D). Thus, it would have been obvious to one skilled in the art at the time the invention was made to modify the invention of Hosoya with the p-type layer, as taught by Nakamura, so as to provide a pn junction diode as claimed.

As to claims 7, 13, Hosoya discloses an active layer 4 of FET 11 (fig. 1) which is separated from the active layer 4 of the diode 12 (fig. 1).

#### *Response to Arguments*

4. Applicant's arguments filed April 01, 2005, have been fully considered but they are not persuasive.

In the remarks, applicant contends that the newly amended claims overcome the prior rejection. In particular, the newly added limitation states “at least one ion implanted region disposed between the field effect transistor and the pn junction diode. On the contrary, Nakamura et al. discloses that limitation, as discussed in the above rejection.

According to the above rejection, Hosoya discloses the invention substantially as claimed. However, Hosoya does not explicitly disclose that the diode is a pn junction diode having a p-type layer and an n-type layer. Nakamura discloses an analogous semiconductor device, the device (fig. 11D and fig. 12) having a pn junction diode (col. 4, lines 14-15; fig. 11D) with a p-type layer 306 and an n-type layer 303 (col. 4, lines 20-21). The diode includes a cathode and an anode (col. 4, lines 4-8; and col. 3, lines 65-68). Further, the device includes at least one ion implanted region 304, 302 (fig. 11D) disposed between the field effect transistor 309 (fig. 11D) and the pn junction (fig. 11D). Therefore , it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Hosoya with the pn diode having a p-type layer and an n-type layer and at least one ion implanted region, as taught by Nakamura, so as to improve the breakdown voltage of the diode (Nakamura, col. 1, lines 25-27).

For the foregoing reasons, the rejection is maintained.

**Conclusion**

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

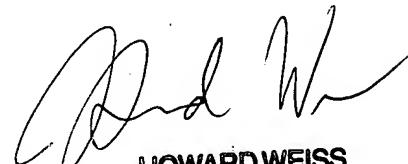
Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Vikki Trinh whose telephone number is (571) 272-1719. The Examiner can normally be reached from Monday-Friday, 9:00 AM - 5:30 PM Eastern Time. If attempts to reach the examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Wael Fahmy, can be reached at (571) 272-1705. The office fax number is 703-872-9306.

Any request for information regarding to the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Also, status information for published applications may be obtained from either Private PAIR or Public PAIR. In addition, status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. If you have questions

pertaining to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site ([www.uspto.gov](http://www.uspto.gov)), from the Office of Public Records and from commercial sources. Applicants are referred to the Electronic Business Center (EBC) at <http://www.uspto.gov/ebc/index.html> or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

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PRIMARY EXAMINER